A Single-Chip Transceiver for 802.11a and Hiperlan2 Wireless LANs

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Abstract — **A fully integrated transceiver for 802.11a and Hiperlan2 wireless local area network applications is described. This single-chip transceiver employs direct conversion with on-chip channel-select filters and DC offset cancellation servo circuitry, as well as correction loops for maintaining accurate I/Q balancing and transmitter power control. The transceiver exceeds both WLAN standard requirements for the 54 Mbps mode, demonstrating a receiver sensitivity of –75 dBm for this mode. A highly flexible interface allows a variety of baseband processors to interface with this chip.**

I. INTRODUCTION

The recent proliferation of WLAN technology in the 2.4 GHz ISM band has caused a demand for more channels and network throughput. This demand is addressed by the IEEE 802.11a standard [1] in the US and by ETSI BRAN Hiperlan2 [2] in Europe. Both standards operate in the 5-6 GHz license-free bands and use very similar physical layer, as they are both based on OFDM (orthogonal frequency division multiplexing) modulation and support data rates of up to 54 Mbps.

In this paper we present a single-chip direct-conversion radio transceiver that is designed to meet the requirements of both standards and supports the 54 Mbps mode. The transceiver block diagram is shown in Fig. 1. The interface to the chip has been flexibly designed to accommodate a variety of baseband processors. The transmitter, receiver and synthesizer blocks are now discussed.

II. TRANSMITTER

In the transmit chain differential I and Q signals are directly up-converted to the desired channel by a direct conversion mixer, consisting of a differential-input I/Q modulator based on a current-commutating technique. The up-converted 5 GHz signal is passed through a gain control block consisting of two identical voltage-controlled amplifiers. This block supports more than 45 dB of transmit power control as required by the Hiperlan 2 standard [2]. The gain in dB of this amplifier chain is linearly controlled by an external analog DC voltage.

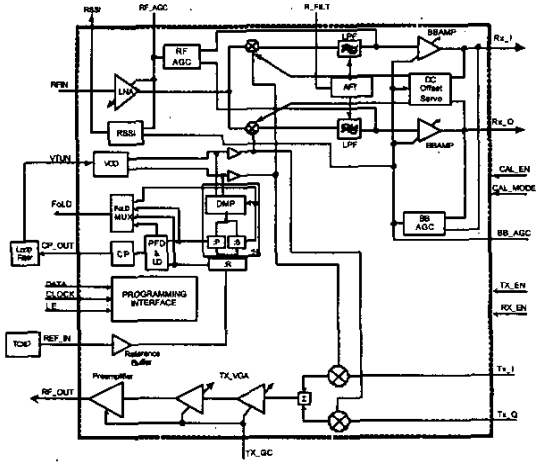

Fig. 1 Block diagram of the 5 GHz transceiver.

The transmitter is capable of delivering +4 dBm undistorted OFDM signal power (+14 dBm 1-dB compression point). The transmitter chain is fully balanced in order to reduce the effects of parasitic signal coupling from the substrate and the power supply. The nominal voltage gain of the transmitter is 13 dB.

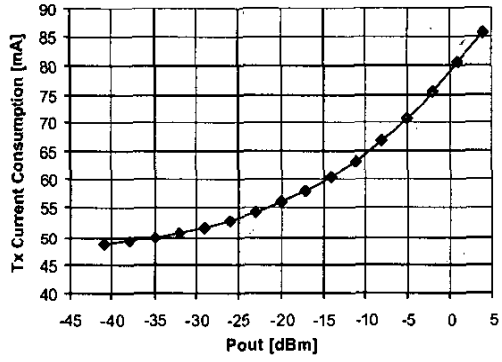

Fig. 2 Tx chain current consumption vs. output power.

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The power consumption of the variable gain stage and the preamplifier is controlled by the transmitter's gain control voltage, providing a power saving feature during low-power transmissions, as shown in Fig. 2. This yields a power consumption reduction for the transmit chain of up to 45% when the gain changes over a 45 dB output power range.

III. SYNTHESIZER

The synthesizer comprises a low-noise quadrature VCO, a dual-modulus prescaler, a high precision charge pump, an external loop filter and all necessary digital logic. The control of the frequency synthesizer is performed via a 3-wire serial interface.

The VCO operates in the lower and middle bands of the 802.11a and the lower band of the Hiperlan 2 wireless LAN standards between 5.15 and 5.35 GHz. It consists of two identical bipolar common-base Colpitts LC oscillators using on-chip inductors. The two VCOs are coupled through transconductors, which force them to oscillate in quadrature.

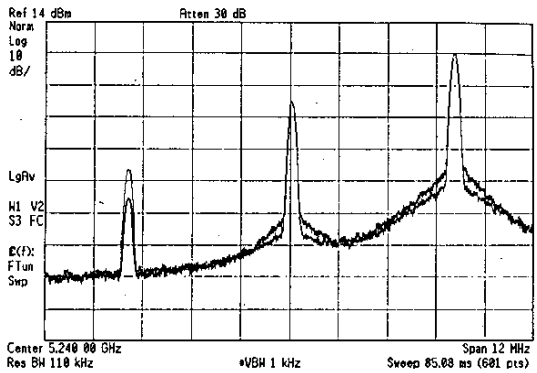

Fig. 3 Improvement on SSB rejection when the synthesizer's correcting loops are engaged.

Quadrature errors coming from layout parasitics, device mismatches and any unwanted coupling are compensated with the aid of on-chip phase and amplitude correcting loops, employing high-frequency phase and amplitude detectors. Fig. 3 shows the performance improvement in sideband rejection when the correcting loops are engaged and the transmitter is setup as a SSB modulator. The transmitter achieves 45 dB of sideband rejection.

The variable divider in the feedback path consists of a 32/33 dual-modulus prescaler followed by a programmable divider. The prescaler design is based on an 8/9 shift register divider followed by two divide-by-two stages. The VCO is phase-locked to a reference frequency that can be 5, 10 or 20 MHz to accommodate all the channels in the 5 GHz WLAN bands. The loop also includes a conventional phase-frequency detector with programmable delay in the reset path in order to mitigate the dead zone effect.

IV. RECEIVER

The receiver employs direct down-conversion architecture with on-chip channel-select filters and DC offset cancellation servo circuitry. Additionally, the receiver includes two self-contained AGC loops controlling the gain of the LNA and the baseband amplifiers; this simplifies the interfacing requirements between the RF transceiver and the baseband chip. Alternatively, the two AGC loops can close externally through a baseband processor, should one decide to use proprietary baseband algorithms. An on-chip RSSI circuit provides signal strength indication to the baseband processor.

The low-noise amplifier (LNA) is implemented as a differential structure in order to reduce the effects of parasitic signal coupling from the substrate and the power supply. The input impedance of the LNA is 100 O differentially. The gain of the LNA is tunable in a 30 dB range through a DC control voltage produced by the RF AGC block, which senses the total signal strength at the output of the low-pass filters, including both in-band signal and residual interferer signals. This gain control is achieved using a "current steering" technique. When the AGC loop is closed, the RF AGC circuitry forces the filters' composite output RMS value to be equal to a level programmable through the serial interface.

The IQ down-converter translates the RF signal directly to baseband I and Q streams. It consists of two current-commutating mixers (Gilbert cells) that provide current output, thus allowing proper operation at low supply voltages.

The baseband I and Q streams are fed to on-chip channel-select low-pass filters, which provide most of the adjacent and alternate channel rejection required by the 802.11a and HiperLan 2 standards [1]-[2]. These filters have a 5th-order low-pass Chebyshev response with 0.08 dB ripple. They are implemented using the MOSFET-C technique. This technique makes possible a lower excess noise factor in comparison to Gm-C filters. The value of the MOSFET resistors is tightly controlled by an automatic frequency tuning block, which uses an external resistor as reference.

The output of each of the filters is fed to a baseband amplifier, implemented using a transconductor feeding a transimpedance amplifier [3]; this configuration provides

adequate bandwidth for this application. The gain of each baseband amplifier is tunable in a 60 dB range through a DC voltage produced by the baseband AGC block. The gain in dB is a linear function of this control voltage. When the AGC loop is closed, the baseband AGC circuitry forces the baseband amplifiers' composite output RMS value to be equal to a level programmable through the serial interface.

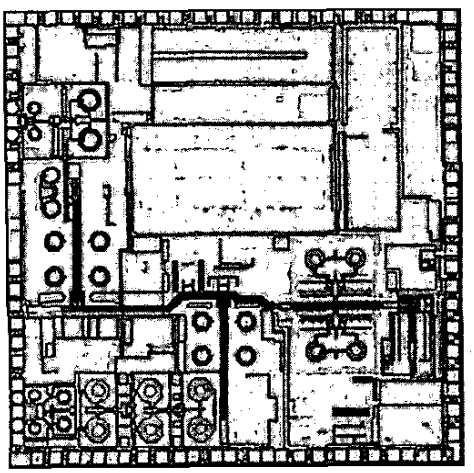

Fig. 4 Die microphotograph

In order to reduce the DC offset produced by the direct conversion technique, a DC servo loop is used from the output of the baseband amplifiers to the output of the mixer. When the loop is closed, the baseband chain exhibits a high-pass behavior, with a corner frequency set by two external capacitors. The residual DC offset is measured to be less than 30 mV.

The operation of the AGC and DC offset calibration loops provides very fast calibration during the synchronization preamble specified by the standards. Only two signals are necessary for the control of these loops. These signals provide gating of the calibration as well as differentiation between the two standards in order to provide optimal performance. The fast behavior of the AGC and DC offset loops provides a convergence time of less than 4 microseconds.

V. MEASURED RESULTS

The transceiver chip was fabricated in a 0.5 um SiGe BiCMOS process. A chip microphotograph is shown in Fig. 4. The chip area is 16 mm^2. Extensive measurements have been performed. Fig. 5 shows the measured transmitted OFDM spectrum showing spectral images at -41 dBr at ±20 MHz and -46 dBr at ±40 MHz and a RF carrier leakage -5 dB relative to the average power of the rest of the subcarriers. Fig. 6 shows the measured Tx EVM (Error Vector Magnitude); an EVM of 29 dB at the maximum output power of 4 dBm can be seen. Fig. 7 shows the phase noise performance of the synthesizer. The close-in phase noise is at -91 dBc while the integrated phase noise over the 10 kHz to 1 MHz bandwidth is 1.8 degrees.

The receiver exhibits an overall noise figure of 5.5 dB and achieves −75 dBm sensitivity in the 54 Mbps mode and -92.5 dBm for the 6 Mbps mode assuming that 18.5 dB and 1 dB of SNR respectively are required to achieve a PER of 0.1. The on-chip channel selection filter provides 20 dB adjacent channel rejection and 60 dB alternate channel rejection. The input-referred 1 dB compression point is at -6 dBm. Fig. 8 shows the performance of the receiver in terms of EVM versus input power.

Table I summarizes the typical measured performance of the chip.

VI. CONCLUSIONS

A single-chip transceiver for 802.11a and Hiperlan2 wireless LANs has been described. This transceiver makes extensive use of servo loops for maintaining accurate performance of the transmitter and receiver blocks. Power control in the transmitter makes possible energy savings during quiet transmit periods. The design achieves a high degree of integration and a highly flexible interface to baseband processors.

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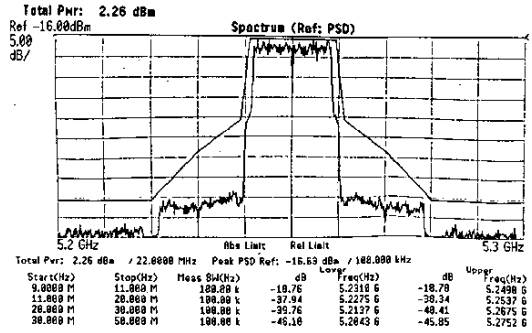

Fig. 5 Transmit spectrum at +4 dBm output power.

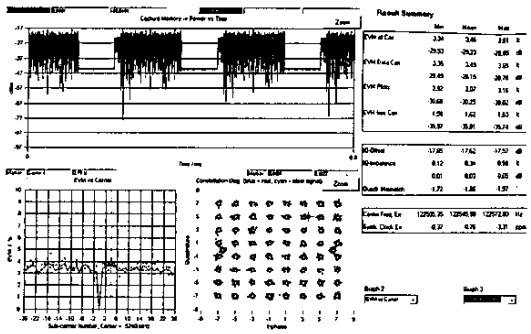

Fig. 6 Transmitter EVM performance.

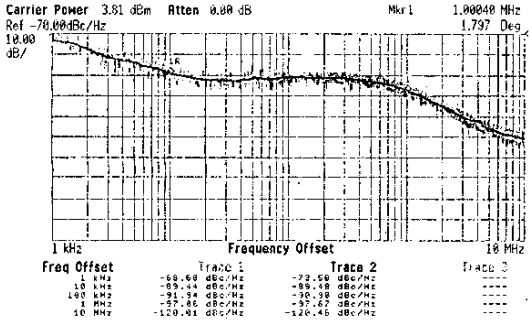

Fig. 7 Synthesizer phase noise.

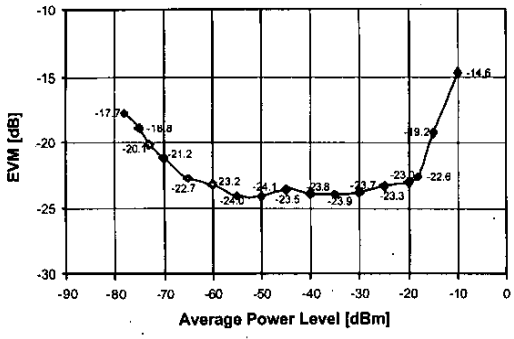

Fig. 8 Receiver EVM performance vs. input power level.

TABLE I
MEASURED PERFORMANCE SUMMARY

Supply Voltage	3 V
Tx chain current consumption	86 mA at +4 dBm P_{out}
Rx chain current consumption	98 mA
Synthesizer current consumption	60 mA
Tx output power	4 dBm
Tx 1 dB compression point	14 dBm
Tx gain control range Close-in phase noise	>45 dB -91 dBc
Rx noise figure	5.5 dB
Rx 1 dB compression point	-6 dBm
Adjacent channel rejection	20 dB
Alternate channel rejection	60 dB